AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A method of controlling an output buffer circuit for generating an output signal and outputting the output signal from an output terminal, wherein the output buffer circuit includes a first drive circuit for receiving an input signal, and a second drive circuit connected to the output terminal ~~and having a lower output impedance than the first drive circuit~~, the method comprising the steps of:

generating a first output signal having a first state in accordance with the input signal using the first drive circuit, wherein the first state indicates one of a high logical level and a low logical level; and

driving the second drive circuit to generate a second output signal having the first state by a driving signal which is generated by adding a predetermined delay to the output signal.

2. (Currently Amended) A method of controlling an output buffer circuit comprising first and second drive circuits, the first drive circuit including a first output transistor connected between a first power supply and an output terminal of the output buffer circuit and a second output transistor connected between a second power supply and the output terminal, the second drive circuit including a third output transistor connected between the first power supply and the output terminal and a fourth output transistor connected between the second power supply and the output terminal~~, the third and fourth output transistors having lower impedances than the first and second output transistors~~, the method comprising the steps of:

generating a first output signal having a first state in accordance with the input signal using the first drive circuit, wherein the first state indicates one of a high logical level and a low logical level;

generating a delay signal by delaying the output signal;

generating a control signal for controlling the third and fourth output transistors in accordance with the delay signal and the input signal; and

driving the second drive circuit to generate a second output signal having the first state by the control signal.

3. (Previously Presented) The method according to claim 2, wherein the first output signal generating step includes generating the first output signal by turning on the first output transistor;

the driving step includes turning on the third output transistor with the control signal; and

the method further comprises a step of substantially simultaneously turning off the first and third output transistors in accordance with a change in the input signal.

4. (Previously Presented) The method according to claim 2, wherein the first output signal generating step includes generating the first output signal by turning on the second output transistor;

the driving step includes turning on the fourth output transistor with the control signal; and

the method further comprises a step of substantially simultaneously turning off the second and fourth output transistors in accordance with a change in the input signal.

5. (Currently Amended) An output buffer circuit comprising:

a first drive circuit, connected to an output terminal, for receiving an input signal and generating a first output signal having a first state indicative of one of a high logical level and a low logical level;

a second drive circuit connected to the output terminal ~~and having a lower output impedance than the first drive circuit~~, wherein the second drive circuit generates a second output signal; and

a first control circuit, connected to the second drive circuit, for generating a first control signal for driving the second drive circuit on the basis of the input signal and a delay signal which is generated by adding a predetermined delay to the first output signal such that the second drive circuit generates the second output signal having the first state.

6. (Previously Presented) The output buffer circuit according to claim 5, wherein the first drive circuit includes a first output transistor connected between a first power supply and the output terminal and a second output transistor connected between a second power supply and the output terminal, wherein the first and second output transistors generate the first output signal; and

the second drive circuit includes a third output transistor connected between the first power supply and the output terminal and a fourth output transistor connected between the second power supply and the output terminal, the third and fourth output transistors having lower impedances than the first and second output transistors.

7. (Previously Presented) The output buffer circuit according to claim 6, wherein the first control circuit turns on the third output transistor with the first control signal after the first output transistor is turned on by the input signal, and the first control circuit turns on the fourth output transistor with the first control signal after the second output transistor is turned on by the input signal.

8. (Original) The output buffer circuit according to claim 6, further comprising a second control circuit, connected to the first drive circuit, for inverting the input signal to generate second and third control signals respectively supplied to the first and second output transistors, wherein the first control circuit generates the first control signal and a fourth control signal that have phases opposite to a phase of the input signal and are respectively supplied to the third and fourth output transistors.

9. (Original) The output buffer circuit according to claim 6, further comprising a second control circuit, connected to the first drive circuit, for generating second and third control signals respectively supplied to the first and second output transistors, wherein the first control circuit generates the first control signal and a fourth control signal respectively supplied to the third and fourth output transistors.

10. (Original) The output buffer circuit according to claim 5, wherein the second drive circuit includes a plurality of sub -drive circuits having different impedances, wherein at least one of the sub-drive circuits is selectively enabled to set the output impedance of the second drive circuit.

11. (Previously Presented) The output buffer circuit according to claim 10, wherein the first control circuit supplies the first control signal to each of the sub-drive circuits based on the input signal, the delay signal and a select signal.

12. (Withdrawn) An output buffer circuit comprising:

first and second output transistors connected in series between a first power supply and a second power supply;

first and second control circuits, connected to the first and second output transistors, for receiving an input signal and respectively generating first and second control signals for controlling the first and second output transistors, wherein the first and second output transistors generate an output signal at an output terminal of the output buffer circuit; and

a third control circuit, connected between the output terminal and the first and second control circuits, for receiving the input signal and the output signal and controlling a slew rate of the output signal by controlling slew rates of the first and second control signals in accordance with the input signal and the output signal, wherein the third control circuit controls the first and second control circuits when the first and second output transistors are turned off to generate the first and second control signal in accordance with the input signal, and controls the first and second control circuits when the first and second output transistors are turned on such that the first and second control signals sharply rise or fall in response to a change in the input signal, gently rise or fall after a predetermined time elapses, and thereafter sharply rise or fall when the output signal reaches a predetermined level.

13. (Withdrawn) The output buffer circuit according to claim 12, wherein the first and second control circuits respectively include first and second switching elements and first and second resistor elements respectively connected in parallel to the first and second switching elements; and

the output buffer circuit further comprises a delay circuit, connected to the third control circuit, for generating a delay signal by delaying the input signal,

wherein when the first and second output transistors are turned on, the third control circuit controls the first and second control circuits in accordance with the delay signal and the output signal such that the first and second control signals are generated by turning on and off the first and second switching elements.

14. (Withdrawn) The output buffer circuit according to claim 13, wherein the third control circuit includes:

a first inverter circuit, connected to the output terminal and having a relatively low threshold voltage, for receiving the output signal and generating a first inverted signal;

a second inverter circuit, connected to the output terminal and having a relatively high threshold voltage, for receiving the output signal and generating a second inverted signal;

a NAND gate, connected to the delay circuit and the first inverter circuit, for receiving the delay signal and the first inverted signal and generating a first switching control signal for controlling the first switching element; and

a NOR gate, connected to the delay circuit and the second inverter circuit, for receiving the delay signal and the second inverted signal and generating a second switching control signal for controlling the second switching element.

15. (Withdrawn) The output buffer circuit according to claim 13, wherein the third control circuit includes:

a Schmitt inverter circuit, connected to the output terminal and having a hysteresis characteristic, for receiving the output signal and generating an inverted output signal;

a NAND gate, connected to the delay circuit and the Schmitt inverter circuit, for receiving the delay signal and the inverted output signal and generating a first switching control signal for controlling the first switching element; and

a NOR gate, connected to the delay circuit and the Schmitt inverter circuit, for receiving the delay signal and the inverted output signal and generating a second switching control signal for controlling the second switching element.

16. (Withdrawn) An output buffer circuit comprising:

first and second output transistors connected in series between a first power supply and a second power supply;

first and second control circuits, respectively connected to the first and second output transistors, for receiving an input signal and respectively generating first and second control signals for controlling the first and second output transistors, wherein the first and second output transistors generate an output signal that is output from an output terminal of the output buffer circuit in response to the first and second control signals, the first and second control circuits respectively including first and second switching elements and first and second resistor elements respectively connected in parallel to the first and second switching elements; and

a third control circuit, connected between the output terminal and the first and second control circuits, for receiving the input signal and the output signal and controlling a slew rate of the output signal by controlling slew rates of the first and second control signals in accordance with the input signal and the output signal, the third control circuit including,

a first inverter circuit, connected to the output terminal and having a relatively low threshold voltage, for receiving the output signal and generating a first inverted signal,

a second inverter circuit, connected to the output terminal and having a relatively high threshold voltage, for receiving the output signal and generating a second inverted signal,

a NAND gate, connected to the first inverter circuit, for receiving the input signal and the first inverted signal and generating a first switching control signal for controlling the first switching element, and

a NOR gate, connected to the second inverter circuit, for receiving the input signal and the second inverted signal and generating a second switching control signal for controlling the second switching element.

17. (Withdrawn) An output buffer circuit comprising:

first and second output transistors connected in series between a first power supply and a second power supply;

first and second control circuits, respectively connected to the first and second output transistors, for receiving an input signal and respectively generating first and second control signals for controlling the first and second output transistors, wherein the

first and second output transistors generate an output signal that is output from an output terminal of the output buffer circuit in response to the first and second control signals, the first and second control circuits respectively including first and second switching elements and first and second resistor elements respectively connected in parallel to the first and second switching elements; and

a third control circuit, connected between the output terminal and the first and second control circuits, for receiving the input signal and the output signal and controlling a slew rate of the output signal by controlling slew rates of the first and second control signals in accordance with the input signal and the output signal, the third control circuit including,

a Schmitt inverter circuit, connected to the output terminal and having a hysteresis characteristic, for receiving the output signal and generating an inverted output signal,

a NAND gate, connected to the Schmitt inverter circuit, for receiving the input signal and the inverted output signal and generating a first switching control signal for controlling the first switching element, and

a NOR gate, connected to the Schmitt inverter circuit, for receiving the input signal and the inverted output signal and generating a second switching control signal for controlling the second switching element.

18. (Withdrawn) A semiconductor device comprising:

an output buffer circuit including,

first and second output transistors connected in series between a first power supply and a second power supply,

first and second control circuits, connected to the first and second output transistors, for receiving an input signal and respectively generating first and second control signals for controlling the first and second output transistors, wherein the first and second output transistors generate an output signal output from an output terminal of the output buffer circuit in response to the first and second control signals, and

a third control circuit, respectively connected between the output terminal and the first and second control circuits, for receiving the input signal and the output signal and controlling a slew rate of the output signal by controlling slew rates of the first and second control signals in accordance with the input signal and the output signal, wherein the third control circuit controls the first and second control circuits when the first and second output transistors are turned off to generate the first and second control signal in accordance with the input signal, and controls the first and second control circuits when the first and second output transistors are turned on such that the first and second control signals sharply rise or fall in response to a change in the input signal, gently rise or fall after a predetermined time elapses, and thereafter sharply rise or fall when the output signal reaches a predetermined level.

19. (Previously Presented) The method according to claim 1, wherein the first output signal generating step includes generating the first output signal that has a gentle waveform in accordance with an input signal having a sharp waveform.

20. (Previously Presented) The method according to claim 2, wherein the first output signal generating step includes generating the first output signal that has a gentle waveform in accordance with an input signal having a sharp waveform.

21. (Previously Presented) The output buffer circuit according to claim 5, wherein the first drive circuit receives an input signal having a sharp waveform and generates the first output signal that has a gentle waveform.

22. (Previously Presented) The output buffer circuit according to claim 5, further comprising a delay circuit, connected to the output terminal, for delaying the first output signal and generating a delayed output signal.

23. (Currently Amended) A method of controlling an output buffer circuit comprising first and second drive circuits, the first drive circuit including a first output transistor of a first type and a second output transistor of a second type, the second drive circuit including a third output transistor of the first type and a fourth output transistor of the second type~~, the third and fourth output transistors having lower impedances than the first and second output transistors~~, the method comprising the steps of:

generating a first output signal having a first state in accordance with the input signal by turning on the first transistor of the first date circuit, wherein the first state indicates one of a high logical level and a low logical level; and

driving the second drive circuit to generate a second output signal having the first state by turning on the third transistor of the second drive circuit by a driving signal which is generated by adding a predetermined delay to the first output signal.

24. (Previously Presented) The method according to claim 23, wherein the first output signal generating step includes generating the first output signal that has a gentle waveform in accordance with an input signal having a sharp waveform.

25. (Currently Amended) An output buffer circuit comprising:

a first drive circuit including a first transistor of a first type and a second output transistor of a second type which are connected to an output terminal, wherein the first and second transistors receive an input signal and generate a first output signal having a first state by turning and generating a first output signal having a first state by turning on the first transistor or the second transistor, wherein the first state indicates one of a high logical level and a low logical level;

a second drive circuit including a third transistor of the first type and a fourth transistor of the second type which are connected to the output terminal, ~~wherein the third and fourth output transistors have lower impedances than the first and second output transistors~~; and

a first control circuit, connected to the second drive circuit, for generating a first control signal for turning on the third transistor on the basis of the input signal and a delay signal which is generated by adding a predetermined delay to the first output signal such that the second drive circuit generates a second output signal having the first state.

26. (Previously Presented) The output buffer circuit according to claim 25, wherein the first drive circuit receives an input signal having a sharp waveform and generates the first output signal that has a gentle waveform.

27. (Previously Presented) The output buffer circuit according to claim 25, further comprising a delay circuit, connected to the output terminal, for delaying the first output signal and generating a delay output signal.

28. (Currently Amended) A method of controlling an output buffer circuit for generating an output signal and outputting the output signal from the output terminal, wherein the output buffer circuit includes a first drive circuit for receiving an input signal, and a second drive circuit connected to the output terminal ~~and having a lower output impedance than the first drive circuit~~, the method comprising the steps of:

generating a first output signal having a first state in accordance with the input signal using the first drive circuit, wherein the first state indicates one of a high logical level and a low logical level;

monitoring whether the first output signal is changed by a predetermined amount; and

driving the second drive circuit to generate a second output signal having a first state when monitoring that the first output signal is changed by a predetermined amount.

29. (Currently Amended) An output buffer circuit comprising:

a first drive circuit, connected to an output terminal, for receiving an input signal and generating a first output signal having a first state indicative of one of a high logical level and a low logical level;

a second drive circuit connected to the output terminal ~~and having a lower output impedance than the first drive circuit~~ for generating a second output signal; and

a first control circuit connected to the second drive circuit for monitoring whether the first output signal is changed by a predetermined amount and generating a first control signal when monitoring that the first output signal is changed by a predetermined amount, wherein the first control signal drives the second drive circuit such that the second drive circuit generates the second output signal having the first state.

30. (New) The method of claim 1, wherein the second drive circuit has a lower output impedance than the first drive circuit.

31. (New) The method of claim 2, the third and fourth output transistor having lower impedances than the first and second output transistors.

32. (New) The output buffer circuit of claim 5, wherein the second drive circuit has a lower output impedance than the first drive circuit.

33. (New) The output buffer circuit of claim 23, wherein the third and fourth output transistors have lower impedances than the first and second output transistors.

34. (New) The output buffer circuit of claim 25, wherein the third and fourth output transistors have lower impedances than the first and second output transistors.

35. (New) The method of claim 28, wherein the second drive circuit has a lower output impedance than the first drive circuit.

36. (New) The output buffer circuit of claim 29, the second drive circuit has a lower output impedance than the first drive circuit.

37. (New) An output buffer circuit comprising:

a fist drive circuit disposed between a high power supply voltage and a low power supply voltage and connected to an output terminal, for receiving an input signal and generating a first output signal having one of the high power supply voltage and the low power supply voltage;

a second drive circuit connected to the output terminal for generating a second output signal; and

a first control circuit, connected to the second drive circuit, for generating a first control signal that drives the second drive circuit on the basis of the input signal and a control signal which is generated by adding a predetermined delay to the first output signal such that the second drive circuit generates the second output signal having the same power supply voltage as that of the first output signal.